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| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | 6 |

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/976,707 | DORSEY, MICHAEL C. |
| | Examiner | Art Unit |
| | John P Trimmings | 2133 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☒ Claim(s) *35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☑ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/Mar. 03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-36 are presented for examination.

### *Information Disclosure Statement*

The examiner has considered the applicant's Disclosure Statements of 3/27/2003.

### *Drawings*

1. The drawings are objected to because:

   a. FIG.2 LSSD and STEP CLKS are not referred to in the disclosure.

   b. FIG.9 LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SDCAN_CLKB are not referred to in the disclosure.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Specification*

2. The disclosure is objected to because of the following informalities:

   a. Page 5 line 28 recites "synchronous random access memory ("SRAMs")". The statement is a combination of two terms; "Static Random Access Memory, an SRAM", and "Synchronous Dynamic Random Access Memory, an SDRAM", the terms of which are generally accepted in the

art. The examiner suspects that the applicant wishes to recite a "static random access memory", but would like the applicant to respond as to the device type specifically intended. Appropriate correction is required.

b. The disclosure is objected to because of the following informalities: page 7 line 15 describes engine 110 being configured by a 66 bit signal composed of a 32 bit vector and 33 bit seed. The sum of 32 and 33 is not 66. Appropriate correction is required.

c. The disclosure is objected to because of the following informalities: page 10 line 1 recites, "(bits $B_{26}$ to $B_0$)", but the examiner believes that it should read, "(bits $B_{30}$ to $B_0$)". Appropriate correction is required.

d. The disclosure is objected to because of the following informalities: page 10 line 11 recites, "LBST_STEP_STEPE", but the examiner cannot find this reference in FIG.9. Appropriate correction is required.

e. The disclosure is objected to because of the following informalities: page 10 line 19 recites, "components 150", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

f. The disclosure is objected to because of the following informalities: page 11 line 28 and 31, page 14 line 7 recite, "ASIC 100", but the examiner cannot find this reference in the drawings, and believes it should read "ASIC 150". Appropriate correction is required.

g. The disclosure is objected to because of the following informalities: page 13 line 8 recites, "initialized them to...", but the examiner believes it

should read "initialized to...". Appropriate correction is required.

### *Claim Objections*

3. Claim 35 is objected to because of the following informalities: the examiner believes that line 2 should recite "machine" in the singular. The examiner also suggests that the applicant change the word "includes" in line 2 to "comprises". Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 4, 14 and 27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims specify using a "paranoid check" for a purpose within a MBIST signature register. The same term is mentioned in the disclosure but the term was never defined. The examiner, being one with ordinary skill in the art, is unsure of what the applicant means when using this term.

5. Claim 28 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter, which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The performing of a LBIST utilizing the reset memory state machine was not disclosed in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 4, 14 and 27are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "paranoid check" in claims 7 and 28 is used by the claim to mean a test which the examiner is not familiar, while the accepted meaning is "to check again by another means." The term is indefinite because the specification does not clearly redefine the term.

7. Claim 26 recites the limitation "the dual mode built-in self-test controller" in line 4. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-4, 7-9, 11-14 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al., U.S. Patent No. 5982189.

As per Claim 1:

Motika et al. teaches a built-in self-test controller (FIG.2 50), comprising: a plurality of alternative memory built-in self-test state machines (FIG.2 32); and a memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines (FIG.2 32 and column 3 lines 38-63).

As per Claim 2:

Motika et al. teaches the built-in self-test controller of claim 1(FIG.2 50), further comprising a logic built-in self-test engine (FIG.2 34).

As per Claim 3:

Motika et al. teaches the built-in self-test controller of claim 1 (FIG.2 50), further comprising a memory built-in self-test signature generated by an execution of the memory built-in self-test (column 3 lines 56-60).

As per Claim 4:

Motika et al. teaches the built-in self-test controller of claim 3, wherein the memory built-in self-test signature includes the results of at least one paranoid check. Since the examiner is unsure of the meaning of "paranoid check" (see 35 USC 112(1) and 112(2) rejections), it is assumed that the signature register of Motika et al. includes results of this kind (column 3 lines 39-63).

As per Claim 7:

Motika et al. teaches a built-in self-test controller (FIG.2 50), comprising: means for implementing a plurality of states in a plurality of sets in a memory built-in self-test (column 2 lines 63-65); and means for operating a predetermined one of the sets in the memory built-in self-test (column 4 lines 6-8).

As per Claim 8:

Motika et al. teaches the built-in self-test controller of claim 7, further comprising a logic built-in self-test engine (FIG.2 34 and column 3 lines 39-42).

As per Claim 9:

Motika et al. teaches the built-in self-test controller of claim 7, further comprising a memory built-in self-test signature generated by an execution of the memory built-in self-test (column 3 lines 5660).

As per Claim 11:

Motika et al. teaches an integrated circuit device (column 1 lines 5-9), comprising: a plurality of memory components (FIG.2 36); a testing interface (FIG.2 60), and a built-in self-test controller controlled through the testing interface (FIG.2 50),

comprising: a plurality of alternative memory built-in self-test state machines (FIG.2 32); and a memory built-in self-test engine (FIG.2 32) operating a predetermined one of the memory built-in self-test state machines.

As per Claim 12:

Motika et al. teaches the integrated circuit device of claim 11, further comprising a logic built-in self-test engine (FIG.2 34).

As per Claim 13:

Motika et al. teaches the integrated circuit device of claim 11, further comprising a memory built-in self-test signature register generated by an execution of the memory built-in self-test (column 3 lines 56-60).

As per Claim 14:

Motika et al. teaches the integrated circuit device of claim 13, wherein the memory built-in self-test signature includes the results of at least one paranoid check. Since the examiner is unsure of the meaning of "paranoid check" (see 35 USC 112(1) and 112(2) rejections), it is assumed that the signature register of Motika et al. includes results of this kind (column 3 lines 39-63).

As per Claim 19:

Motika et al. teaches an integrated circuit device (column 1 lines 5-9), comprising: a plurality of memory components (FIG.2 36); a testing interface (FIG.2 60); and a built-in self-test controller controlled through the testing interface (FIG.2 50), comprising: means for implementing a plurality of states in a plurality of sets in a

memory built-in self-test (FIG.2 32 and column 4 lines 6-8); and means for operating a predetermined one of the sets in the memory built-in self-test (column 4 lines 6-8).

As per Claim 20:

Motika et al. teaches the integrated circuit device of claim 19, further comprising a logic built-in self-test engine (FIG.2 34).

As per Claim 21:

Motika et al. teaches the integrated circuit device of claim 19, further comprising a memory built-in self-test signature register generated by an execution of the memory built-in self-test (column 3 lines 53-60).

9. Claims 25, 29, 30 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Kraus et al., U.S. Patent No. 6587979.

As per Claim 25:

Kraus et al. teaches a feature for performing a built-in self-test on an integrated circuit device (see Abstract), comprising: externally resetting a predetermined one of a plurality of memory state machines in a memory built-in self-test controller (column 9 lines 52-58); performing a memory built-in self-test utilizing the reset memory state machine (column 9 lines 58-67); and obtaining the results of the performed memory built-in self-test (column 10 lines 55-61).

As per Claim 29:

Kraus et al. teaches the feature of claim 25, wherein obtaining the results includes receiving the results as the memory built-in self-test is performed (column 10 lines 61-67).

As per Claim 30;

Kraus et al. teaches a feature for testing an integrated circuit device (see Abstract), comprising: interfacing the integrated circuit device with a tester (column 9 lines 24-26 and FIG.5 21); externally resetting a built-in self-test controller (column 9 lines 52-58), including: externally resetting a predetermined one of a plurality of memory state machines (column 9 lines 52-67); performing a memory built-in self-test from the built-in self-test controller (column 9 lines 52-67 and column 10 lines 1-3); obtaining the results of the performed memory built-in self-test (column 10 lines 55-61).

As per Claim 36:

Kraus et al. teaches the feature of claim 30, wherein obtaining the results includes receiving the results as the memory built-in self-test is performed(column 10 lines 61-67).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 5, 15, 18 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189 as applied to claim 3, 11 and 13 above, in view of Au et al., U.S. Patent No. 6681359.

As per Claims 5 and 15:

The controller of Claim 3 or 13 is further limited whereas the signature includes a "done" bit. Au et al., in column 9 line 25-33 defines such a feature. And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within an MBIST while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claims are rejected.

As per Claim 18 and 24:

The device of Claim 11 or 19 is further limited whereas the interface is a JTAG tap controller. Au et al., in FIG.3 112 and in the Abstract teaches such an arrangement, and in view of the motivation for Au et al. elsewhere, the claim is rejected.

11. Claims 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, as applied to Claims 11 and 19 above, in view of Kim et al., U.S. Patent No. 6148426. As per the objection to the disclosure above (paragraph 2a above), the examiner believes that since there does not appear to be a "synchronous random access memory" in the art, the examiner assumes that the applicant wishes to recite "static random access memory" in the subject claims. These

claims therefore limit the memory device to being a "static random access memory". In an analogous art, Kim et al. teaches an MBIST (see Abstract) that is used for testing an SRAM (see Title). Citing a savings in BIST size and cost (column 2 lines 55-61), Kim et al. would motivate one with ordinary skill in the art at the time of the invention to combine the art for the purpose of testing SRAM memories.

12. Claims 6 and 10 and 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189 as applied to claim 1 and 7 and 11 and 19 above, in view of Zuraski Jr. et al., U.S. Patent No. 6560740, and further in view of Lo et al., U.S. Patent No. 5661732. The claims, dependent on Claim 1 or 7 or 11 or 19 above, further limit the controller wherein the state machine comprises a reset state entered upon an external reset signal (Zuraski et al, column 10 lines 31-36). However Zuraski et al. does not further limit the machine to flushing and testing. In an analogous art, Lo et al., upon entering a 1$^{st}$ state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (Lo et al. column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (Lo et al. FIG.1 26). In Zuraski et al., a better BIST for functionally testing memories is discussed, and in Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Zuraski et al. and Lo et al., would combine the references, and so the claims are rejected.

13. Claims 26, 27, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979, and in view of Lo et al., U.S. Patent No. 5661732.

As per Claims 26 and 31:

The claim, dependent on Claim 25 or 30 above, further limit the features wherein a state is entered upon to initialize the MBIST. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (Lo et al. column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (Lo et al. FIG.1 26). One with ordinary skill in the art at the time of the invention, motivated by Lo et al. as previously stated, would combine the references, and so the claims are rejected.

As per Claims 27 and 32:

The claims, dependent on Claim 26 or 31above, further limit the features wherein the results of a paranoid test is stored in the MBIST signature register. Since the examiner is unsure of the meaning of "paranoid check" (see 35 USC 112(1) and 112(2) rejections), it is assumed that the signature register of Kraus et al. includes results of this kind (column 10 lines 55-61). Therefore, in view of the prior motivation, the calims are rejected.

14. Claims 28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979 as applied to Claim 25 and 30 above, and in view of Motika et al., U.S. Patent No. 5982189.

As per Claim 28:

The feature of Claim 25 is further limited wherein the external reset of Kraus et al. (column 9 lines 52-58) is performed on the logic machine. Since this claim is also rejected based on 35 USC 112(1), the examiner will assume "logic" when "memory" is stated in the subject claim. In an analogous art, Motika et al. performs an LBIST and then obtains the results (column 3 lines 64-67 and column 4 lines 1-5). And whereas one with ordinary skill in the art at the time of the invention, motivated to perform a BIST with built-in stress testing (column 1 lines 64-67), would combine the references, thus the claim is rejected.

As per Claim 33:

The feature of Claim 30 is further limited wherein obtaining the results includes reading a signature register. Motika et al., in column 3 lines 56-60 supports such a feature, and in view of the prior motivation for Motika et al., the claim is rejected.

15. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979 as applied to claim 30 above, and in view of Au et al., U.S. Patent No. 6681359. The feature of Claim 30 is further limited whereas the interface is a JTAG tap controller. Au et al., in FIG.3 112 and in the Abstract teaches such an arrangement, and in view of the motivation for Au et al. elsewhere, the claim is rejected.

16. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979 as applied to claim 30 above, and in view of Arimilli et al., U.S. Patent No. 6665828. The feature of Claim 30 is further limited whereas the resetting of the BIST includes resetting an LBIST, further performing an MBIST. Kraus et al. performs the MBIST as per Claim 30, but does not reset an LBIST. In an analogous art, Arimilli et al. in column 6 lines 7-31 performs such a task. And, as Arimilli et al. describes a better way to test ever-larger circuits without increasing test circuit size (column 1 lines 1-67 and column 2 lines 1-6), one with ordinary skill in the art at the time of the invention, motivated by Arimilli et al., would combine the references, and so the claim is rejected.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
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Albert DeCady
Primary Examiner